Course Description

Course name	**#053 - Mastering Power Integrity with Signal Integrity and EMC Foundations**
Duration	5 **days**
Format	**Public Classroom, Inhouse Event and Online**

Overview

Dr. István Novák, Principal Signal and Power Integrity Engineer, Samtec, Boston, USA, is teaching this unique 5-day course focuses on **Power Integrity, PI** with a broad and unified outlook to **Signal Integrity, SI** and **EMC**. It shows that not only the underlying physics, but also many design rules are essentially the same across these disciplines, and the seemingly contradictory rules are the result of different initial conditions.

The course is based on forty years of teaching, research and successful industrial design experience. It shows working and proven design practices and pitfalls to avoid. It will illustrate live HW and SW demonstrations, ranging from a variety of home-made tools to professional commercial HW and SW.

This course is a must for system board and package designers, power engineers and their managers as well as for silicon designers who want to understand the application environment of their chips.

Technical Focus

Power integrity, PI, has emerged as the latest and still growing challenge for electronic designs, as the landscape for the three disciplines Signal Integrity, Power Integrity and Electromagnetic Compatibility has shifted. While **signal integrity, SI**, and electromagnetic compatibility, **EMC**, still pose challenges, their disciplines and the possible pitfalls and their solutions have been more widely studied and understood. Power noise, and its impact on SI and EMC, on the other hand, creates daily new challenges and their solutions are still being worked out. Whether it is component characterization or high-speed channel link budgeting, the power integrity tasks can not be successfully solved without taking into account the signal integrity and EMC principles.

This unique course focuses on PI with a broad and unified outlook to SI and EMC. It shows that not only the underlying physics, but also many design rules are essentially the same across these disciplines, and the seemingly contradictory rules are the result of different initial conditions.
The course is based on forty years of teaching, research and successful industrial design experience. It shows working and proven design practices and pitfalls to avoid. It will illustrate live HW and SW demonstrations, ranging from a variety of home-made tools to professional commercial HW and SW.
This course is a must for system board and package designers, power engineers and their managers as well as for silicon designers who want to understand the application environment of their chips.

Course Content

This unique course provides a unified analysis and design approach to the power-integrity, signal-integrity and electromagnetic compatibility disciplines with the main focus on power distribution network design, validation, testing and simulations. It emphasizes the most recent challenges that the

digital and mixed analog/digital designers face, with time devoted to signal integrity analysis, design methods, solutions and component selection.
We will deal with the underlying physical rules with minimal mathematics. With interactive software and live hardware and software demo illustrations, the various good and bad design choices are explained, and trade-offs are shown for achieving high-performance yet cost-effective designs. Among others, the course shows why PI requires the impedance, whereas SI requires scattering parameters for their designs and validation processes.

Participants will learn how bit error rate (BER) and jitter depend on power noise, how to analyse and minimize their effects. You will also learn the surprising fact that conductor surface roughness is actually more detrimental for low-frequency power distribution than for high-speed signaling. We also show the counter-intuitive fact that current distribution in conductors is not uniform even at DC, resulting in geometry-dependent extra losses.

The course provides an overview of power distribution design methodologies and shows that worst-case power noise and worst-case high-speed eye closure can be calculated based on the same principles. Cost-effective PCB stackup, material and component choices are discussed together with simulation and measurement solutions for power distribution networks and high-speed signaling. The course also shows how to select, characterize and measure DC-DC converters and power filters.

Participants will receive several of the tools and simulation files shown in the class as well as the book **Power Distribution Design Methodologies.** There is an option to purchase the book Frequency-Domain Characterization of Power Distribution Networks at a special discount, available only to course participants.

Who should attend?
The course is aimed at engineers, scientists and managers facing signal integrity challenges in electronics designs for the computer, communications, consumer, medical, defense or automotive industries.

Only basic understanding of electronic circuits is assumed because the course is delivered through practical illustrations and examples and emphasizes the understanding of the underlying physics.

Whether you are already knowledgeable in circuit design or in the theory of signal integrity, you will find many useful tidbits and a solid explanation of the signal-integrity discipline.

Course Daily Schedule

This course will mostly discuss power integrity, but with emphasized and specific outlooks to signal integrity and EMC.

A series of dedicated hardware (HW) and software (SW) illustrations and design examples will show and explain the underlying physical phenomena and major design rules of proper design.

Day one
Common Foundation of Power Integrity, Signal Integrity and EMC

- How signal spectrum is related to PI, SI and EMC requirements?
- When do you need time or frequency-domain solutions?
- Commonalities and differences between power planes and signal traces
- Characteristic impedance, delay, matching and termination solutions and rules
- Understanding impedance and scattering matrices for PI and SI use
- Parasitics of RLC components, how to interpret catalogue data and how to create accurate simulation models for power and signal integrity

Examples, live HW and SW demos: Calculation of interconnect parameters, reflection, matching, signal bandwidth and spectra

Day two
Multi-Line, Loaded and Lossy Interconnects

- Printed circuit board construction rules, laminate selection; how material properties impact PI, SI and EMC
- The various types of crosstalk in power and signal networks
- Crosstalk reduction, crosstalk metrics in time and frequency domain
- Differential Interconnects, effects of imbalance, interpreting and calculating mixed-mode S parameters and mode conversion
- Effect of electrical loading and discontinuities on power planes and signal traces
- Designing for multi-rail power distribution and multi-line signal crosstalk, simultaneous switching noise
- DC drop on planes, DC power distribution, minimizing voltage drop by proper connections

Examples, live HW and SW demos: Effect of capacitive loading on power planes and transmission bandwidth, designing for a specific crosstalk goal

Day Three
System Design

- When do we need single-point or multi-point grounding?
- Grounding options in mixed-mode applications
- Shielding and electromagnetic interference rules and solutions
- Skin loss, dielectric loss, surface roughness, laminate and copper selection, through holes and blind/buried Vias, bends, stubs
- Clock distribution, skew, jitter, jitter separation, relation to bit error rate (BER) and power noise
- Clock sources and drivers, clock PLLs, spread-spectrum Clocking in signaling and power distribution
- Jitter tolerance and jitter transfer
- Inter symbol interference in power and signal integrity, Reverse Pulse Technique and Peak Distortion Analysis; linear network solutions of passive interconnects

Examples, live HW and SW demos: Termination and resonances in power planes and Clock networks

Day four
Power Distribution Design Methodologies

- DC-DC converters, transient response, output impedance, loop stability
- Lumped PDN Design, the Target Impedance concepts and its proper use
- Synthesizing PDN impedance: pros and cons of multi-pole, big-V and other design strategies
- Bypass capacitor selection and placement, service area of capacitors
- Connecting the charge time-of-flight and target-impedance concepts
- Multi-node PDN Design
- Proper design of power filters

Examples, live HW and SW demos: Simulation of bypass capacitor service area, output impedance and gain-phase plots of DC-DC converters

Day five
Signal and Power Integrity Measurements and Modelling

- Creating simulation models for DC-DC converters, bypass components, high-speed interconnects
- Simulating vias, planes, bypass capacitors, DC-DC converter stability and output impedance
- Major challenges and their solutions in power and signal-integrity measurements

Examples, live HW and SW demos: Measuring very low impedances reliably and accurately, filter design and performance

Instructor Biography

Dr. István Novák. Principal Signal and Power Integrity Engineer, Samtec, Boston, USA.

Dr. Novák is a Life Fellow of IEEE for his contributions to signal-integrity modeling, measurements and simulations. He has 40+ years of experience in high-speed and high-power electronics designs as well as teaching and consulting. He is the lead-author of the book "Frequency Domain Characterization of Power Distribution Networks", published in 2007, and the executive editor of the book "Power Distribution Design Methodologies," published in 2008. He is invited technical blogger on the EDN, SI-Journal and PCB007 websites.

At Samtec, he is currently working on new technologies that enable customers to improve power delivery and increase data speeds beyond 100Gbps.

Until 2018 he was with Oracle, Boston, where he was leading and mentoring a team of signal and power-integrity engineers at Oracle doing 10 - 25 Gbp passive-channel characterization, designs and modeling, as well as power distribution and new technology developments for high-performance server platforms.

During the past twenty years he has been doing the high-speed power-integrity and signal-integrity designs of SUN's and Oracle's successful T5, T3, T2000, T1000, V880, V490, V440 midrange server families. He developed signal-integrity and power-integrity strategies, simulation, measurement and validation procedures. He introduced the industry's first super-thin laminates into volume-produced server PCBs and drove several industry cooperations to improve power distribution and bypassing technologies. He was SUN's representative on the InfiniBand Cable and Connector Workgroup.

Previously Dr. Novák advised the European Laboratory for Particle Physics (CERN) on signal-integrity and EMC issues for Fibre Channel data-collection systems of the Large Hadron Collider.

Dr. Novák had his technical education from the Technical University of Budapest, and his Ph.D. degree from the Hungarian Academy of Sciences. He organized and led the High Speed Technology Team at the Technical University of Budapest, where his teaching activity covered transmission lines and wave propagation, communications systems, EMC and signal-integrity issues of high-speed designs.

He holds twenty-five patents in the field of power distribution, signal integrity, precision measurements and digital signal processing, and published over one hundred technical papers. **DesignCon 2020 honors Dr. István Novák as 2020 Engineer of the Year!** Dr. Novák's homepage.

Dr. Novák has been a member of the Continuing Education Institute-Europe faculty since 1992.