Course Description

Course name	**#054 - Signal and Power Integrity: Advanced High-Speed Design and Characterization**
Duration	5 **days**
Format	**Public Classroom, Inhouse Event and Online**

Overview

Dr. István Novák, Principal Signal and Power Integrity Engineer, Samtec, Boston, USA, is teaching this 5-day course in advanced high-speed design and characterization.

With machine learning and artificial intelligence needs on the rise, the thousands of amperes currents on some of the power rails create unique challenges across our designs, manufacturing and validation. Properly designed power distribution is a key requirement to achieve good signal integrity and to avoid electro-magnetic interference problems.

As companies are working towards data rates over 400 Gbps and main-stream serial signaling is in the 5-10 Gbps range; signal rise and fall times shrink to single digit picoseconds.
As a result of these signal and power integrity trends, laminate and copper characteristics, glass-weave effects and surface roughness, frequency-dependent trace and component parameters, inter-symbol interference (ISI), jitter and finite bit-error-rate (BER) all need to be re-evaluated and reconsidered. With the increasing utilization of equalization and pre-emphasis, validations even with eye diagrams may not be sufficient.

Today, equally challenging is the proper design of power distribution. A multitude of supply voltages, shrinking target impedance values approaching tens of microohms and higher channel attenuations come with reduced timing and noise margins. The allowed noise on signals and on supply rails decreases and the increasing density and bandwidth of interconnects inter-link the previously independent power-integrity, signal-integrity and EMC design domains. Also, the mere definition of impedance on a power rail with tens of microohms impedance becomes non-trivial.

Technical Focus

Power distribution is becoming an increasing challenge in today's electronic designs, small and big alike. Properly designed power distribution is essential also for good signal integrity and to avoid electro-magnetic interference problems.

Parallel memory bus speeds of 4800 to 5200MHz are becoming main-stream, GDDR7 is using 32Gbps signaling, high-end communications gears moving rapidly beyond 112 Gbps transfer speeds; signal rise and fall times shrink to below 10 ps.

As a result, laminate and copper characteristics, surface roughness, glass-weave effects and glass structure, frequency-dependent trace and component parameters, material and structural anisotropy, inter-symbol interference (ISI), jitter and finite bit-error-rate (BER) all need to be considered. With the dominant utilization of equalization and pre-emphasis, validations even with masks and eye diagrams may not be sufficient, giving way to Channel Operating Margin (COM) and Effective Return Loss (ERL) and a slew of statistical aggregated crosstalk definitions.

Today, equally challenging is the proper design of power distribution. A multitude of different supply voltages and signaling levels come with reduced timing and noise margins. The allowed noise on signals and on supply rails decreases and the increasing density and bandwidth of interconnects inter-link the previously independent power-integrity, signal-integrity and EMC design domains.

Course Content

This thoroughly updated and renewed unique course is based on decades of successful design experience of satellite circuits and high-end computer systems. It provides a unified analysis and design approach to the power-integrity and signal-integrity disciplines with a brief overview of EMI-prevention tasks in modern digital systems that are necessary to understand the proper signal- and power-integrity design approaches. After a brief summary of basic concepts, the course focuses on the most recent challenges that the digital and mixed analog/digital designers face, with an increased portion devoted to proven power distribution analysis techniques, design methods, solutions and practical details of component selection. The course deals with the underlying physical rules with minimal mathematics. With interactive software and live hardware and software demo illustrations, the various good and bad design choices are explained, and trade-offs are shown for achieving high-performance yet cost-effective designs.

For power distribution and EMC, the course explains the benefits and proper use of impedance profile of the bypass network, how it relates to time-domain design and validation methods and how to estimate and compare the worst-case transient noise of various PDN synthesis techniques. Long-haul crosstalk among different power domains, simulation and measurement solutions for PDN impedances in the tens of microohms are discussed. The key elements of long-term reliability and foundations of robust yet cost-effective designs are explained. For high-speed signal transmission, emphasis is put on the dispersive, potentially anisotropic and lossy nature of PCB and package traces showing the link between rise-time degradation, jitter, eye closure and the frequency-dependent dielectric constant, dielectric loss tangent and copper surface roughness. Link performance is explained in terms of S parameters, Channel Operating Margin and Effective Return Loss.

Who should attend?

Participants will receive a free copy of the popular book “Power Distribution Design Methodologies” and several of the illustration tools and simulation files shown in the class.

The course is aimed at engineers, scientists and managers facing the combined signal- and power-integrity challenges in electronics designs for the computer, communications, consumer, medical, defense or automotive industries.

Only basic understanding of electronic circuits is assumed, because the course is delivered through practical illustrations and examples and emphasizes the understanding of the underlying physics.

Whether you are already knowledgeable in circuit design or in the theory of signal and power integrity, or new to these topics, you will find many useful tidbits and a solid explanation of the important disciplines.

Course Daily Schedule

Day 1,
Common Foundation of Signal and Power Integrity

- Introduction to signal and power integrity
    - Comparing signal spectra, time and frequency-domain solutions for SI and PI
- Reflections, matching, terminations
    - Characteristic impedance, phase and group delay, termination solutions
- Time and frequency domain solutions, linear networks
    - What we need to know about S and Z matrices
- Printed circuit board manufacturing and construction options, core and foil construction, HDI and HDI+
    - The art of selecting a good stackup
    - What are the important parameters for SI and PI

Examples, live HW and SW demos: Calculation of interconnect parameters, reflection, matching, bandwidth and spectra of SI signals and power noise

Day 2,
Crosstalk and Loaded Interconnects

- Crosstalk and crosstalk-reduction in signal and power integrity
    - Metrics in time and frequency domain
- Differential interconnects
    - Effects of imbalance, mixed-mode S parameters, mode conversion
- Effect of electrical loading and discontinuities
    - Bandwidth and rise-time impact of loading on high-speed traces and power planes
- Discrete R-L-C components
    - Critical design parameters and reliability considerations: DC and AC bias, temperature coefficient

Examples, live HW and SW demos: Effect of capacitive loading on transmission bandwidth, designing for a specific crosstalk goal

Day 3,
Losses, Discontinuities and PDN Design

- Conductive and dielectric losses, vias, discontinuities, via shield
- How roughness impacts signal and power integrity, laminate selection, via models
- Grounding, shielding and the basic EMI rules
- PDN design methodologies
    - The Reverse Pulse Technique, pros and cons of the Big-V, Multi-pole and Flat impedance synthesis
    - Ways to minimize transient noise
- DC power distribution
    - DC drop on planes, why sharp turns are bad at DC, too

Examples, live HW and SW demos: Termination and quarter- and half-wave resonances in signal channels and clock networks

Day 4,
Power Distribution Design Details

- Power converters and sources
    - Switching and linear regulators, batteries, transient response, output impedance, loop stability
- PDN components and filters
    - Filter design process, most of the time the appropriate transfer function is not Z21 or S21
- Mid- and high-frequency bypassing with power-ground laminates
    - Inductance of vias, planes, selecting and connecting bypass capacitors

Examples, live HW and SW demos: Simulation of bypass capacitor service area, output impedance and gain-phase plots of DC-DC converters

Day 5,
Signal and Power Integrity simulations, Measurements and Modelling

- S-parameter models, simulations and de-embedding procedures
    - Field solvers and circuit simulators
    - Full-wave, Quasi-TEM and lumped models
    - Connecting N-port S parameter blocks, challenges with fixture deembedding
- High power and high frequency measurement techniques
- Time-domain and frequency-domain measurements: which is better?

- How to ensure proper VNA measurements up to 100+ GHz
- Setups and accessories to measure sub-milliohm impedances
    - The resilience of two-port shunt-through connection

Examples, live HW and SW demos: Anatomy of PDN resonances, reducing ground loop impact on signal- and power-integrity measurements

Instructor Biography

Dr. István Novák. Principal Signal and Power Integrity Engineer, Samtec, Boston, USA.

Dr. Novák is a Life Fellow of IEEE for his contributions to signal-integrity modeling, measurements and simulations. He has 40+ years of experience in high-speed and high-power electronics designs as well as teaching and consulting. He is the lead-author of the book "Frequency Domain Characterization of Power Distribution Networks", published in 2007, and the executive editor of the book "Power Distribution Design Methodologies," published in 2008. He is invited technical blogger on the EDN, SI-Journal and PCB007 websites.

At Samtec, he is currently working on new technologies that enable customers to improve power delivery and increase data speeds beyond 100Gbps.

Until 2018 he was with Oracle, Boston, where he was leading and mentoring a team of signal and power-integrity engineers at Oracle doing 10 - 25 Gbp passive-channel characterization, designs and modeling, as well as power distribution and new technology developments for high-performance server platforms.

During the past twenty years he has been doing the high-speed power-integrity and signal-integrity designs of SUN's and Oracle's successful T5, T3, T2000, T1000, V880, V490, V440 midrange server families. He developed signal-integrity and power-integrity strategies, simulation, measurement and validation procedures. He introduced the industry's first super-thin laminates into volume-produced server PCBs and drove several industry cooperations to improve power distribution and bypassing technologies. He was SUN's representative on the InfiniBand Cable and Connector Workgroup.

Previously Dr. Novák advised the European Laboratory for Particle Physics (CERN) on signal-integrity and EMC issues for Fibre Channel data-collection systems of the Large Hadron Collider.

Dr. Novák had his technical education from the Technical University of Budapest, and his Ph.D. degree from the Hungarian Academy of Sciences. He organized and led the High Speed Technology Team at the Technical University of Budapest, where his teaching activity covered transmission lines and wave propagation, communications systems, EMC and signal-integrity issues of high-speed designs.

He holds twenty-five patents in the field of power distribution, signal integrity, precision measurements and digital signal processing, and published over one hundred technical papers. **DesignCon 2020 honors Dr. István Novák as 2020 Engineer of the Year!** Dr. Novák's homepage.

Dr. Novák has been a member of the Continuing Education Institute-Europe faculty since 1992.