Course Description

Course name	**#055 - Signal Integrity: Advanced High-Speed Design and Characterization**
Duration	5 **days**
Format	**Public Classroom, Inhouse Event and Online**

Overview

Dr. István Novák, Principal Signal and Power Integrity Engineer, Samtec, Boston, USA, is teaching this 5-day course in **Signal Integrity**: **Advanced High-Speed Design and Characterization**.

High-speed designs continue to undergo major technology changes. In recent years, parallel memory signalling rates are above 1000 Mbps and main-stream serial signalling is in the 5-10 Gbps range; signal rise and fall times shrink to way below 10 ps.

As a result, **laminate and copper characteristics**, glass-weave and surface roughness, frequency-dependent trace and component parameters, inter-symbol interference (ISI), jitter and finite bit-error-rate (BER) all need to be understood and taken into account during the design process.

With the increasing utilization of transmit and receive equalizations, validation even with eye diagrams measured at package pins may not be sufficient in itself. Today, equally challenging is the proper design of power distribution. A multitude of supply voltages and signalling levels come with reduced timing and noise margins.

The allowed noise on signals and on supply rails decreases and the increasing density and bandwidth of interconnects eventually link the previously independent power-integrity, signal-integrity and **EMC design** domains.

Technical Focus

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Course Content

This course uses a series of dedicated hardware (HW) and software (SW) illustrations and design examples to show and explain the underlying physical phenomena and major design rules of proper signal-integrity design.

The course gives guidance to properly select medium- and low-loss laminates, stackup and layout to ensure good signal integrity without expensive over-design.

The class focuses on signal integrity in board and system interconnects with the necessary brief overview of EMC design principles. Detailed power-integrity design and validation is covered in the companion course #56; Power Integrity: Advanced Design and Characterization. The HW and SW illustrations are shown live during the class.

The teaching methodology is based on showing and explaining good and bad design choices, discussing pros and cons of options and focusing on manufacturability and robust performance.

The course is taught with minimal mathematics, relying on the physical phenomena and a few easy-to-remember basic rules. For high-speed signal transmission, emphasis is put on the dispersive and lossy nature of cables, PCB and package traces, glass-weave, copper roughness, showing the link between rise-time degradation, jitter, eye closure and the frequency-domain scattering and transfer parameters. For power distribution and EMC, emphasis is put on the proper impedance profile of the bypass network and how to estimate and compare the worst-case transient noise of various design methodologies.

Case studies and simple exercises make the learning experience complete.

Participants will receive several of the tools and simulation files shown in the class.

Who should attend?

The course is aimed at engineers, scientists and managers facing signal integrity challenges in electronics designs for the computer, communications, consumer, medical, defense or automotive industries.

Only basic understanding of electronic circuits is assumed because the course is delivered through practical illustrations and examples and emphasizes the understanding of the underlying physics.

Whether you are already knowledgeable in circuit design or in the theory of signal integrity, you will find many useful tidbits and a solid explanation of the signal-integrity discipline.

Course Daily Schedule

Day 1

Single and Multiple Unloaded Interconnects

- Signal Spectrum, Time and Frequency-domain Solutions
- Characteristic Impedance, Delay and Performance Regions of Interconnects
- Matching and Termination Solutions and Rules; Allowable Mismatch
- Time and Frequency Domain Solutions, Network Matrices, What You Need to Know About S Parameters
- PCB Construction Rules, Stackup Options and Limitations, Cost and Reliability Considerations

Examples, live HW and SW demos: Calculation of Interconnect Parameters, Reflection, Matching, Signal Bandwidth and Spectra

Day 2

Differential, Multi-Line Interconnects

- Crosstalk in the Time and Frequency Domain, Stackup and Laminate Dependance
- Crosstalk reduction, Shield Traces, Shield Resonance
- Differential Interconnects, Effects of Imbalance, Routing Skew, Mixed-mode S Parameters, Mode Conversion, Glass-weave Effects
- Design for Multi-line Crosstalk, Simultaneous Switching Noise
- Multi-drop and Point-to-point Interconnect Characteristics, Loaded-line Periodical Filtering

Examples, live HW and SW demos: Effect of Capacitive Loading on Transmission Bandwidth, Designing for a Specific Crosstalk Goal

Day 3

Lossy and Dispersive Interconnects

- Parasitics of RLC Components, Integrated Passives
- Skin Loss, Dielectric Loss, Surface Roughness, Laminate Choice and Selection - How low-loss laminates can hurt us
- Discontinuities, Through Holes and Vias, Bends, Stubs, Design Limits
- Via Construction and Characteristics, Pad, Antipad, Drill-Size Selection
- Grounding, Shielding and EMI Rules, Dangers of Poor Cable Shielding

Examples, live HW and SW demos: Calculating Losses, How to Read S Parameters and Interpret the Impulse Response

Day 4

System Design

- Clock Sources and Drivers, Clock PLLs, Spread-spectrum Clock
- Clock Distribution, Skew, Jitter, Layout and Power-supply Rules to Minimize Jitter
- Jitter Tolerance and Jitter Transfer
- ISI, Eye Diagram, Peak Distortion Analysis, Linear Network Solutions
- Cascading High-speed Interconnect Building Blocks, S Parameters and Transfer Matrices
- Component Placement, Stackup and Layout Optimization

Examples, live HW and SW demos: Termination and Resonances in Clock Networks, Transmit and Receive Equalization, Eye Diagrams

Day 5

Simulation, Measurement, Validation

- Simulating and Modelling Vias, Planes, Bypass Capacitors
- Rules for Creating and Validating Simulation Models
- Rules to Select Simulation Tools, Settings and Setups
- Signal-integrity Simulation Pros and Cons, Simulating with S Paramenters
- Selecting Probes, Cables and Instruments for Signal-integrity Measurements
- Characterization and Validation of High-speed Systems

Examples, live HW and SW demos: Anatomy of Simulation Accuracy, Probes, Cables and Instrumentation Options

Instructor Biography

Dr. István Novák. Principal Signal and Power Integrity Engineer, Samtec, Boston, USA.

Dr. Novák is a Life Fellow of IEEE for his contributions to signal-integrity modeling, measurements and simulations. He has 40+ years of experience in high-speed and high-power electronics designs as well as teaching and consulting. He is the lead-author of the book "Frequency Domain Characterization of Power Distribution Networks", published in 2007, and the executive editor of the book "Power Distribution Design Methodologies," published in 2008. He is invited technical blogger on the EDN, SI-Journal and PCB007 websites.

At Samtec, he is currently working on new technologies that enable customers to improve power delivery and increase data speeds beyond 100Gbps.

Until 2018 he was with Oracle, Boston, where he was leading and mentoring a team of signal and power-integrity engineers at Oracle doing 10 - 25 Gbp passive-channel characterization, designs and modeling, as well as power distribution and new technology developments for high-performance server platforms.

During the past twenty years he has been doing the high-speed power-integrity and signal-integrity designs of SUN's and Oracle's successful T5, T3, T2000, T1000, V880, V490, V440 midrange server families. He developed signal-integrity and power-integrity strategies, simulation, measurement and validation procedures. He introduced the industry's first super-thin laminates into volume-produced server PCBs and drove several industry cooperations to improve power distribution and bypassing technologies. He was SUN's representative on the InfiniBand Cable and Connector Workgroup.

Previously Dr. Novák advised the European Laboratory for Particle Physics (CERN) on signal-integrity and EMC issues for Fibre Channel data-collection systems of the Large Hadron Collider.

Dr. Novák had his technical education from the Technical University of Budapest, and his Ph.D. degree from the Hungarian Academy of Sciences. He organized and led the High Speed Technology Team at the Technical University of Budapest, where his teaching activity covered transmission lines and wave propagation, communications systems, EMC and signal-integrity issues of high-speed designs.

He holds twenty-five patents in the field of power distribution, signal integrity, precision measurements and digital signal processing, and published over one hundred technical papers. **DesignCon 2020 honors Dr. István Novák as 2020 Engineer of the Year!** Dr. Novák's homepage.

Dr. Novák has been a member of the Continuing Education Institute-Europe faculty since 1992.