

Course Description

Course name	#056 - Power Integrity: Advanced Design and Characterization
Duration	5 days
Format	Public Classroom, Inhouse Event and Online

Overview

Dr. István Novák, Principal Signal and Power Integrity Engineer, Samtec, Boston, USA, is teaching this 5-day course in **Advanced Design and Characterization**.

Power Distribution Network (PDN) design is becoming one of the biggest design challenges today for systems with increasing speed, power dissipation and density.

A multitude of supply voltages and signalling levels come with reduced timing and noise margins.

The allowed noise on signals and on supply rails decreases and the increasing density and bandwidth of interconnects link the previously independent power-integrity, signal-integrity and Electro-Magnetic Compatibility (EMC) design domains.

Eventually, the power distribution design and characterization becomes a corner stone and enabler for good signal integrity and electromagnetic compatibility. Series filtering for sensitive clock sources, PLLs and SerDes rails require new considerations in component selection.

This course is devoted to power distribution design, simulation & measurement with a brief overview of signal-integrity & electromagnetic compatibility.

Technical Focus

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Course Content

This five-day course is devoted entirely to power distribution design, simulation and measurement with the necessary brief overview of signal-integrity and electromagnetic compatibility principles. Detailed signal-integrity design and validation is covered in the companion course 055 Signal Integrity: Advanced High-Speed Design and Characterization.

The course is based on a large number of hardware (HW) and software (SW) illustrations, shown live during the class. The teaching methodology is based on showing and explaining good and bad design

choices, pointing out potential mistakes, discussing pros and cons of options and focusing on manufacturability and robust performance without costly over-design. The course is taught with minimal mathematics, focusing on the physical phenomena and a few easy-to-remember basic rules.

The course explains the underlying physical rules for successful power distribution designs and shows how the same principles, which can be used to obtain worst-case eye-diagrams in signalling, can also be used to efficiently calculate the worst-case transient noise on power-distribution networks. The course explains the importance of DC drop analysis on power planes, the importance of taking the DC and AC bias characteristics of bypass capacitors and ferrites/inductors.

In the design process, emphasis is put on the proper impedance profile of the bypass network and how to use the impedance profile to estimate and evaluate the worst-case transient noise of various design methodologies. The class answers (among others) such important questions as what stackup and layout details matter for power distribution, how many and what value of bypass capacitors we need, and where to place bypass capacitors for effective noise suppression.

In characterization, equal time is devoted to simulations and measurements. In simulations, different modelling techniques and tools are shown for simulating components, power planes and vias. In measurements, the possible time-domain and frequency-domain instruments are reviewed and the proper set-ups, connections and calibrations are discussed. Participants will receive several of the tools and simulation files shown in the class.

Book Information

A copy of the book "**Power Distribution Design Methodologies**" written by Dr. Novák is handed out to all participants of this course.

Who should attend?

The course is aimed at engineers, scientists and managers facing power integrity challenges in electronics designs for the computer, communications, consumer, medical, defense or automotive industries.

Only basic understanding of electronic circuits is assumed because the course is delivered through practical illustrations and examples and emphasizes the understanding of the underlying physics.

Whether you are already knowledgeable in circuit design or in the theory of power integrity, you will find many useful tidbits and a solid explanation of the power-integrity discipline.

Course Daily Schedule

Day 1

Interaction of Power Integrity, Signal Integrity and Electromagnetic Compatibility

- Waveforms and Spectra of High-speed Signals and Power Noise
- Interaction of Power Integrity, Signal Integrity and Electromagnetic Compatibility
- Grounding and Shielding Rules, PCB Construction Rules, Laminate Choices
- Unified PDN and SI design: Linear Network Analysis, Sources of PDN Noise
- Impulse and Step Responses, Calculating Worst-case Transient Noise

Exercises and illustrations: Signal Spectra, Capacitor Droop and Inductor Current in DC-DC Converters

Day 2

Power Distribution Components

- Characteristics and Parasitics of Various Bypass Capacitor and Inductor Types
- Single Node PDN Design, Impedance Matching
- DC-DC Converter Properties, Transient Response, Output Impedance, Loop Stability
- Selection and Placement of DC-DC Converters
- Designing Filters for Low-current Circuits (SerDes, PLL, Vref)

Exercises and illustrations: Estimating DC-DC Converter Stability, Component Resonances

Day 3

Power Distribution Design Methodologies

- DC Drop on Planes and Traces, Choosing the Proper Geometry for DC Power Distribution
- Determining Copper Weight and Trace Width for Supply Feeds
- High-frequency Bypassing with Power-ground Laminates, Stackup Selection, Thin and Ultra-thin Laminates
- Split Planes and Signal Routing over Splits
- The Procedure of PDN Design, Determining Target Impedance, Point-of-Load PDN Designs from Silicon to DC-DC Converter

Exercises and illustrations: Adding Resistive Voltage Drops, How to Reduce PDN Resonances, PCB Stackup Analysis for PDN

Day 4

Component Selection and Placement through Simulations, Multi-Node Design

- Synthesizing PDN Impedance: Multi-pole, Big-V, DMB Approaches, Stress Distribution, Portability, Sensitivity and Cost Comparison
- High-frequency PDN Design, Service Radius of Bypass Capacitors vs. Matched Planes, How to Handle Multiple Supply Rails in the PDN Design
- How to Identify and Eliminate Capacitor-capacitor and Capacitor-plane Antiresonances, The Role and Impact of Package on PDN Performance
- Lumped Spreadsheet and SPICE PDN Simulations

Exercises and illustrations: Simulation of Bypass Capacitor Service Area, Output Impedance and Gain-Phase Plots of DC-DC Converters

Day 5

Validation of Power Distribution Networks through Measurements

- Frequency-domain Impedance Measurement Set-ups for Milliohm Values: Two-port Shunt-Through Connections
- Where to Measure PDN Noise?
- Why we Should not Measure Noise Across Bypass Capacitors
- Considerations for Sub-system and Full-system PDN Measurements
- Time-domain Measurement Challenges: Uncorrelated External Noise, Dynamic-range Limitations
- How to Select Instruments for PDN Testing

Examples and illustrations: How to Measure Reliably Very Low Impedance Values

Instructor Biography

Dr. István Novák. Principal Signal and Power Integrity Engineer, Samtec, Boston, USA.

Dr. Novák is a Life Fellow of IEEE for his contributions to signal-integrity modeling, measurements and simulations. He has 40+ years of experience in high-speed and high-power electronics designs as well as teaching and consulting. He is the lead-author of the book "Frequency Domain Characterization of Power Distribution Networks", published in 2007, and the executive editor of the book "Power Distribution Design Methodologies," published in 2008. He is invited technical blogger on the EDN, SI-Journal and PCB007 websites.

At Samtec, he is currently working on new technologies that enable customers to improve power delivery and increase data speeds beyond 100Gbps.

Until 2018 he was with Oracle, Boston, where he was leading and mentoring a team of signal and power-integrity engineers at Oracle doing 10 - 25 Gbp passive-channel characterization, designs and modeling, as well as power distribution and new technology developments for high-performance server platforms.

During the past twenty years he has been doing the high-speed power-integrity and signal-integrity designs of SUN's and Oracle's successful T5, T3, T2000, T1000, V880, V490, V440 midrange server families. He developed signal-integrity and power-integrity strategies, simulation, measurement and validation procedures. He introduced the industry's first super-thin laminates into volume-produced server PCBs and drove several industry cooperations to improve power distribution and bypassing technologies. He was SUN's representative on the InfiniBand Cable and Connector Workgroup.

Previously Dr. Novák advised the European Laboratory for Particle Physics (CERN) on signal-integrity and EMC issues for Fibre Channel data-collection systems of the Large Hadron Collider.

Dr. Novák had his technical education from the Technical University of Budapest, and his Ph.D. degree from the Hungarian Academy of Sciences. He organized and led the High Speed Technology Team at the Technical University of Budapest, where his teaching activity covered transmission lines and wave propagation, communications systems, EMC and signal-integrity issues of high-speed designs.

He holds twenty-five patents in the field of power distribution, signal integrity, precision measurements and digital signal processing, and published over one hundred technical papers. **DesignCon 2020 honors Dr. István Novák as 2020 Engineer of the Year!** Dr. Novák's [homepage](#).

Dr. Novák has been a member of the Continuing Education Institute-Europe faculty since 1992.