Course Description

Course name	**#057 - Synchronization and Interconnect in Multiple Clock Domain Systems-on-Chips, SoCs**
Duration	4 **days**
Format	**Public Classroom, Inhouse Event and Online**

Overview
Dr. Reuven Dobkin, CTO of vSync Circuits Ltd. is teaching this 4-day course that explains the Science, Engineering and Art of Synchronization.

Larger and faster **Systems-on-Chips** employ Multiple Clock Domains on the same die for several reasons: Communications with external real-time or pre-defined clocks require chips to incorporate multiple, unrelated clock frequencies; it is more economical in very large chips to break down the system into independently clocked domains, saving some of the power required for clock distribution; and dynamic scaling of voltage and frequency creates multiple clock/voltage domains.

Technical Focus
Larger and faster Systems-on-Chips employ multiple clock domains on the same die for several reasons:

Communications with external real-time or pre-defined clocks require chips to incorporate multiple, unrelated clock frequencies; it is more economical in very large chips to break down the system into independently clocked domains, saving some of the power required for clock distribution; and dynamic scaling of voltage and frequency creates multiple clock/voltage domains.

Interfaces among different clock domains are problematic and are only partly supported by commercial EDA tools.

As a result, synchronization problems are sometimes discovered only in working silicon, and even then, they are hard and expensive to correct.

Course Content
The course teaches the science, engineering and art of synchronization. We define the problems, survey existing solutions, study the best designs, and learn how to select the better synchronizer for each purpose.

We review clocking in digital chips, study the required theoretical basics, learn how to understand synchronization problems, identify them, create reliable solutions, and verify their correctness.

We consider SoC/ASIC and FPGA, mostly at the logical level. Implications on physical design are briefly reviewed. We also review voltage domains, power gating, voltage scaling and their effect on clock domains and synchronization.

Who should attend?
This course is suitable for:

- VLSI/ASIC/SoC/FPGA design engineers,
- architects and managers engaged in the design of advanced SoC VLSI/ASIC/SoC/FPGA
- CAD engineers and developers
- Academic researchers, university professors, and graduate students interested in advanced SoC design

Basic knowledge of digital VLSI/ASIC/FPGA design is assumed. Prior exposure to issues and pitfalls of synchronization is an advantage, but neither
such exposure nor prior knowledge of synchronization is necessary. General background in electrical or computer engineering is useful.

Course Daily Schedule

Clock Distribution Networks

- Problem Definition
- What's Ahead: The technology roadmap
- ASIC/SoC vs. Full-Custom Design Methodologies
- Standard Clock Trees for SoCs and FPGA
- Min-Delay and Max-Delay Problems
- Data Delay Insertion and Delay Line Circuits
- Clock Delay Insertion and Clock Tuning
- Unbalanced Tunable Clock Distribution Networks
- High Performance Clock Trees
- Passive and Active Deskew in Clock Trees
- Local Clock Generation with Tunable Frequencies

Metastability and Synchronization Failures

- Metastability
- Latches and Flip-Flops
- Measuring Metastability
- Probability and MTBF
- Synchronizer Circuits
- Symmetric Booster Synchronizer
- Latency and Settling Time
- Simulating Metastability

Synchronization of Asynchronous Clock Domains

- Control Synchronizers
- Formal Specification Using STG
- Data Validity of Synchronizers
- Push Synchronizers
- Timing Assumptions
- Faster Synchronizers
- Shared Latch Synchronizers
- FIFO Synchronizers
- Reset Synchronization
- Clock Gating and Selection Synchronizers
- Scan Insertion Synchronizer
- Mutual Exclusion and Arbiter

Common Synchronization Errors

- Avoiding Synchronization
- One flop Synchronizers
- Sneaky and Greedy Paths
- Half Protocol
- Async Clear
- Pulse Synchronizers

- Slow-to-Fast Synchronizers
- Metastability Blocker and Filters
- Parallel, Shared Latch, and Conservative
- Synchronizers
- Patented Circuits for Fast Resolution and Pre-Sampling Shaker and Dual Shaker Synchronizers

Verification of Synchronizers

- Identifying Domain Crossings
- Structural Verification
- Sorting the Domain Crossings
- Grouping Synchronizers
- Connecting Bi-Directional Protocols
- Recognizing Synchronizers
- Employing Formal Tools
- Functional Verification
- Data Verification
- Manual Verification

Multi-Synchronous and Periodic Synchronizers

- Mesochronous/Multi-SyncSynchronization
- Delay Variations
- Data Delay Synchronizers
- Conflict Detection
- Clock Delay Synchronizers
- FIFO Synchronizers
- Clock Edge Synchronizers
- Periodic Domains and Predictive Synchronizers

Multi-Synchronous and Asynchronous Long Interconnect

- Definition of Long Interconnects
- Point-to-Point, Buses and Networks on Chip

- Source-Synchronous and Adaptive-Clocked Interconnect
- Data Encoding: Dual rail and 1-of-4
- Four- and Two-Phase Protocols
- Asynchronous Interconnect
- Dual Rail and 1-of-4 Interconnect
- Two-Phase Dual Rail Interconnect
- Fast Serial Interconnect
- Asynchronous and MixedTiming FIFO
- Pipeline Synchronizers
- LDL Synchronizer

Multi-Clock Domain and GALS SoC

- Synchronizer-Based GALS
- Arbitrated and Handshake Stoppable Clocks
- Wrappers and Asynchronous Ports
- GALS Methodologies
- Desynchronization
- Synchronization in Networks on Chips (NoC)

Multiple Voltage Domains

- Definitions, Sources of Multiple Voltages
- Level Shifting and Isolating Gates
- Combining Voltage and Clock Domains
- Floor-Plan and Layout Constraint

Dynamic Voltage and Frequency Scaling

- DVS versus DVFS
- Global versus Multi-Domain Scaling
- Methods of DVFS

Instructor Biography

Dr. Reuven Dobkin received his PhD degree in electrical engineering from Technion, Israel Institute of Technology. Reuven is co-founder of vSync Circuits LTD. (2010), a VLSI EDA and IP company.

Dr. Dobkin worked as a researcher in Technion VLSI Lab, developing novel techniques for on-chip high data rate asynchronous communications. In 2005–2009, Dr. Dobkin worked as VLSI group manager at Ramon Chips LTD., developing Radiation Hardened VLSI technology for space applications. Through the years 1999-2005, Dr. Dobkin worked as project officer in the Armament Research and Development Directory of Ministry of Defense, managing research groups in the fields of VLSI, C4I Systems, Signal Processing and Software Systems Engineering. Beforehand, he led a VLSI design group in IC4IC LTD. developing a family of chips for communications. Through the years 1997-2000 he worked within RAFAEL ASIC Experts design group.

Dr. Dobkin has published numerous papers and holds several patents. He serves as a reviewer of numerous VLSI journals and conferences. His research interests are VLSI architectures, asynchronous logic, synchronization, GALS systems, SoC, NoC and parallel architectures. He has taught a number of industrial courses on synchronization since 2010.

Dr. Dobkin joined Continuing Education Institute-Europe in 2014.