Course Description

Course name	**#075 - Heterogeneous Integration of Chiplets – Defect Inspection, Metrology and Failure Analysis**
Duration	**3 days**
Format	**Public Classroom, Inhouse Event and Online**

Overview

Dr. Ehrenfried Zschech, technical consultant and professor at Brandenburg University of Technology Cottbus-Senftenberg, Germany, is teaching this 3-days course about defect inspection, metrology, and failure analysis in advanced packaging, with the particular focus on materials-related challenges and advanced analytical techniques.

Expand your knowledge of the processing, materials, performance, and reliability aspects of heterogeneous integration of chiplets. Let Professor Zschech guide you all the way from 3D advanced packaging technologies through fault isolation and failure analysis up to the kinetics of degradation processes and reliability challenges. This course will include novel aspects of high-performance computing and AI applications that are driving the demand for increased functionality, performance, and reliability.

Technical Focus

Driven by the consumer's thirst for AI-based applications and the growing market need of advanced electronic products for high-performance computing, semiconductor industry is exploring innovative ways to deliver more functionality in increasingly smaller packages. Three-dimensional (3D) heterogeneous integration and advanced packaging are enabled to extend the promise of Moore's Law and to lower the power consumption. However, ensuring high manufacturing yield and the requested product reliability is challenging. Solder-based 3D-stacking and hybrid bonding require different approaches for metrology, defect inspection and package failure analysis.

Course Content

This course provides an overview of workflows and techniques for defect inspection, metrology, and package failure analysis of advanced microelectronic products. Technology trends and advanced packaging concepts will be discussed. Challenges and needs for fault isolation and failure analysis are addressed, workflows for robust and high-speed defect localization and inspection are discussed. New materials and processes as well as their integration are highlighted, including solutions to achieve high manufacturing yield and to mitigate product reliability issues. The kinetics of thermomechanical and electrical reliability-limiting degradation processes, enforced by package stress, are explained, and ways for effective reliability engineering are shown. The potential of high-resolution 3D X-ray imaging techniques for fault isolation, defect inspection and metrology as well as reliability engineering is emphasized.

Who Should Attend
The goal for this 3-days training course is to help establish a high level of knowledge transfer on fault isolation and package failure analysis of advanced microelectronic products to achieve better understanding of analytical techniques for metrology, defect inspection and physical failure analysis as well as of degradation processes that eventually cause failures. This course is intended for engineers who wish to expand their knowledge in heterogeneous integration and advanced packaging, including concept, technology, materials, performance, and reliability aspects of advanced microelectronic products.

Course Daily Schedule

Day 1: Advanced 3D packaging technologies
– Processes and materials, metrology and defect inspection

1. **Trends in heterogeneous integration and advanced packaging**
   Chiplet architecture and heterogeneous integration is a mega-trend needed for AI-based applications; it is an additional booster for performance and functionality of advanced microelectronic products, e.g. for high-performance computing, and an enabler for less power consumption. Novel technical developments – chiplet architecture, advanced packaging technologies, including hybrid bonding, and the integration of new materials – will be discussed. Roadmaps and market trends for heterogeneous 3D integration and advanced packaging will be shown.

2. **Processes and materials, and their integration**
   Chiplet architectures and their components, designed to achieve high functionality, performance and energy efficiency, will be discussed. Solder microbump/through-silicon-via (TSV) and Cu-Cu hybrid bonding integration schemes, including W2W and D2W technologies, will be shown, and the integration of several new materials will be explained. The categorization of metallurgical contact systems will be done based on metal-physical basics (interdiffusion, intermetallic phase formation and growth), and consequences such as Kirkendall voids and volume change will be explained. This knowledge and the consideration of the properties of the materials that form the contact systems help to achieve high manufacturing yield and to mitigate product reliability issues.

3. **Challenges to metrology and defect inspection**
   Chiplet architectures and their components, designed to achieve high functionality, performance and energy efficiency, will be discussed. Solder microbump/through-silicon-via (TSV) and Cu-Cu hybrid bonding integration schemes and process flows provide different challenges to metrology, e.g. overlay accuracy, and to defect inspection, e.g. the visualization of voids in TSVs, microcracks in solder joints, as well as particles and resulting delamination in

Cu-Cu bonds. The consequences resulting from the continuous scaling down of the feature sizes will be discussed too.

Day 2: Fault isolation and package failure analysis

1. **Specific tasks for 3D-packaged ICs**
   Demanding tasks to physical failure analysis in packaged structures result from the fact that opaque defects have to be localized, imaged and analyzed. This task requires both nondestructive techniques for defect localization and imaging, partially at full-wafer tools in the cleanroom, preparation steps such as deprocessing and cross-sectioning, and destructive detailed analysis of the defect in physical failure analysis labs. Specific tasks for solder microbump/TSV and Cu-Cu hybrid bonding integration schemes and process flows will be explained, and practical examples will be shown.

2. **Workflows for fault isolation and root-cause analysis**
   Workflows for fault isolation and for a final root-cause analysis cover several steps:
   1) electrical fault isolation (EFI) to verify the failing electrical characteristic,
   2) nondestructive imaging using microscopic techniques to visualize the defect,
   3) destructive physical failure analysis techniques to expose and analyze the defect, 4) interpretation of the data and determination of the root cause of the failure.

   Particular focus will be directed on nondestructive imaging techniques for 3D-stacked ICs. Workflows combining several nondestructive techniques such as scanning acoustic microscopy (SAM) and transmission X-ray microscopy (TXM) will be proposed.

3. **Advanced analytical techniques for package failure analysis**
   Analytical techniques for package failure analysis are different to conventional failure analysis in wafer fabs. The need to get 3D information and to visualize buried defects in opaque packages will be demonstrated. In addition to standard failure analysis techniques and tools such as scanning electron microscopy (SEM), transmission electron microscopy (TEM), focused ion beam (FIB) and several diffraction and spectroscopy techniques, nondestructive techniques such as scanning acoustic microscopy (SAM), quantum diamond microscopy (QDM) and transmission X-ray microscopy (TXM) will be explained, and potential and limitations will be discussed.

Day 3: Kinetics of degradation processes and reliability engineering

- **Analytical techniques for in-situ studies**

SEM or TEM imaging of cross-sections through interconnect structures, e.g. prepared mechanically, using laser ablation, or using focused ion beam (FIB) tools, visualize metal structures and defects. However, kinetic studies applying nondestructive characterization techniques are needed for the understanding of degradation processes that eventually cause failure. One technique that has been proven to provide insight into reliability-limiting degradation processes – e.g. electromigration or thermomechanical processes such as microcrack growth – is X-ray microscopy. Nano X-ray **computed** tomography (XCT) and laminography (XCL) reveal 3D information about materials ageing and degradation.

- **Thermomechanical issues and stress-related phenomena**

New performance and reliability challenges caused by design/geometry, processes and materials of 3D stacked ICs will be explained. Particularly, the compatibility of multiple materials with specific properties has to be considered in advanced packaging. Different thermal and mechanical properties of the components, e.g. Young's modulus (E) and coefficient of thermal expansion (CTE), cause thermo-mechanical stress in 3D IC stacks. The packaged-induced thermo-mechanical stress increases the risk of failure caused by delamination along Cu/dielectrics interfaces (adhesive failure) or fracture in dielectrics (cohesive failure). The nondestructive 3D visualization of crack pathways in Cu/low-k interconnect stacks will be shown with nano-XCT.

- **Stress-enforces degradation kinetics and electrical failures**

Electromigration (EM) is a reliability issue for advanced packaging structures and for multilevel on-chip interconnect backend-of-line (BEoL) stacks. Stress-induced effects that enhance the risk to fail for 3D interconnect structures as well as degradation and failure mechanisms connected to 3D stacking of integrated circuits will be explained. The "conventional" degradation processes in BEoL stacks are accelerated by thermomechanical stress, originated from different CTEs of package materials, and time-to-failure is reduced. Electromigration in Cu structures will be explained, including void nucleation, agglomeration, and growth.

Instructor Biography

Professor Dr. Ehrenfried Zschech, Consultant and professor at Brandenburg University of Technology, Cottbus, Germany, is a consultant with hands-on experience in academia and industry. He is providing support throughout the whole supply and innovation chain, particularly in the fields of advanced materials, nanotechnology and microelectronics as well as process control and quality assessment. He holds an adjunct professorship at Faculty of Chemistry of Warsaw University, Poland, as well as honorary professorships for Nanomaterials at Brandenburg University of Technology and for Nanoanalysis at Dresden University of Technology. He has published three books, and he has authored or co-authored more than 300 papers in peer-reviewed journals in the areas of solid-state physics, materials characterization and reliability engineering. Ehrenfried Zschech is Member of the European Academy of Science (EurASc) and Member of the of the German National Academy of Science and Engineering (ACATECH). In 2019, he was awarded the FEMS European Materials Gold Medal.

Ehrenfried Zschech received his Dr. rer. nat. degree from Dresden University of Technology. After having spent four years as a project leader in the field of metal physics and reliability of microelectronic interconnects at Research Institute for Nonferrous Metals in Freiberg, he was appointed as a university teacher for ceramic materials at Freiberg University of Technology. In 1992, he joined the development department at Airbus in Bremen, where he managed the metal physics group and studied the laser-welding metallurgy of aluminum alloys. From 1997 to 2009, Ehrenfried Zschech managed the Materials Analysis Department and the Center for Complex Analysis at Advanced Micro Devices in Dresden. In this position, he was responsible for the analytical support for process control and technology development in leading-edge semiconductor manufacturing, as well as for physical failure analysis. Ehrenfried Zschech was Department Head at the Fraunhofer Institutes IZFP and IKTS and Head of the Steering Committee of the Dresden Fraunhofer Cluster Nanoanalysis from 2009 to 2021. His responsibilities included multi-scale materials characterization and reliability engineering. From 2021 to 2023, he was acting as CTO and Co-Founder of deepXscan GmbH, Dresden, Germany. This start-up company developed and commercialized high-resolution X-ray imaging systems and provided customized solutions for a broad range of applications.

Professor Dr. Zschech has been a member of the Continuing Education Institute-Europe faculty since 2009.