Course Description

Course name	**#088 - Plasma Etching for CMOS Technology and ULSI Applications**
Duration	**4 days**
Format	**Public Classroom, Inhouse Event and Online**

Overview
Dr. Maxime Darnon, at the Laboratoire Hubert Curien in Saint Etienne, France is teaching this 4-day course in Plasma Etching for CMOS Technology and ULSI Applications.

This course is intended to provide an understanding of **plasma processes** for **CMOS applications and ULSI technology.** We will discuss fundamental and practical aspects of front end and back end plasma processes for deep submicron CMOS logic processes.

The course is based on experimental results obtained using commercial etchers connected to very powerful diagnostics of the plasma and the plasma surface interaction.

The discussions cover several aspects of etch processes of materials integrated in advanced CMOS devices, etch mechanisms, and situations that may be encountered for some important plasma processes.

Option 2: Take the short Ecourse **#089 Plasma Etching for Microelectronics Applications.** Combining self-paced e-learning with live weekly sessions with the instructor. Duration in total is two weeks of effective learning. Content based on the first two days of the public course #088

Option 3: Take the full Ecourse **#090 Plasma Etching for Microelectronics Applications: from Fundamental to Practical Applications.** Combining self-paced e-learning with live weekly sessions with the instructor. Duration in total is four weeks of effective learning. Content based on the complete agenda of this course.

Technical Focus
Extensive efforts to miniaturize semiconductor devices is largely attributed to lithography and etching technologies that allow semiconductor thin films patterning in the range of dimensions determined by the semiconductor road map.

During more than 30 years, classical materials, such as aluminum, SiO2, and polysilicon, have been integrated in semiconductor devices.
Nowadays, the technology imposes to work with new materials at each technological node. The integration of new high k and low k dielectric materials, metals at the front and back end of device fabrication, bring on new problem categories.

This imposes the necessity to quickly build up expertise at a rate unprecedented in all the history of semiconductor manufacturing.

Course Content

This course is intended to provide an understanding of plasma processes for CMOS applications and ULSI technology. We will discuss fundamental and practical aspects of front end and back-end plasma processes for deep submicron CMOS logic processes.

The course is based on experimental results obtained using commercial etchers connected to very powerful diagnostics of the plasma and the plasma surface interaction. The discussions cover several aspects of etch processes of materials integrated in advanced CMOS devices, etch mechanisms, and situations that may be encountered for some important plasma processes.

Fundamental parameters obtained from advanced characterizations are used to discuss and analyze plasma etch processes. The emphasis is on real problems, fundamental understanding of processes used in manufacturing, considerations for integration with other steps, and issues brought by the fast device scaling.

Processes covered in detail include silicon gate patterning and all the problems related to critical dimension control as well as results on metal gate and high k dielectric etching. The etch processes associated with the integration of low k materials will be extensively discussed.

Who Should Attend

Any person with a technical background wishing to obtain a better understanding of the mechanistic aspects of plasma-assisted etching, or of reactive gas plasma-surface interactions in general, should benefit from taking this course.

Although the emphasis of the course is on the ULSI circuit fabrication applications, much of the information presented should be of value in the implementation of other processes involving reactive gas plasmas.

A familiarity with the basic concepts of plasma-assisted etching would be helpful but is not essential as the course includes a short summary of the basics.

Course Daily Schedule

Day One

Plasma Fundamentals

- Fundamentals of Cold Plasma Physics
- Plasma Sources used for Etching Application
- Plasma Surface Interactions Involved in Etching

Day Two

Etching Fundamentals

- Pattern Transfer in Plasma Etching
- Profile Control for Plasma Etching
- Monitoring and Controlling a Plasma Etching Processes

Day Three

Plasma Etching for Front End Of Line application

- Photoresist and Mask
- Poly Silicon Gate Etchin
- Metal Gate / High-k Etching
- Atomic Layer Etching
- New Patterning Technologies
- New Transistor Architectures

Day Four

Plasma Etching for Back End Of Line Application

- Etching with a Fluorocarbon-Based Plasma
- Spacers Etching
- Contacts Etching
- Dense SiOCH Etching for Interconnects
- Porous SiOCH Etching for Interconnects
- High Aspect Ratio Structures Etching

Instructor Biography

Dr. Maxime Darnon received his M. Sc. and Ph.D. from Grenoble University, France, in 2007.

Dr. Darnon then worked as a research engineer at IMEC, Leuven, Belgium, and as a research staff member in the advanced plasma group of IBM Research in the T. J. Watson Research Center in Yorktown Heights, NY, USA. His work mostly focused on plasma processes for microelectronics interconnects.

In 2009, he joined the French institute for scientific research (CNRS) as a researcher assigned to the Laboratory of Technologies of Microelectronics (LTM), where he worked on new plasma processes for microelectronics applications.

In 2015, he was assigned to CNRS/LN2 (Laboratory of Nanotechnologies and Nanosystems) at Université de Sherbrooke, Canada, where he used plasma processes to improve solar cells and integrated circuits packaging performance.

Dr. Darnon joined "Laboratoire Hubert Curien" in Saint Etienne, France in 2023 where he today works on micro-nano technologies for optics and photonic applications.

Dr. Darnon is member of the CSTIC, SPIE-AL, PESM and JNTE conference committees and has co-authored more than 100 publications, books, conference proceedings and patents. He is also an elected member of Plasma Science and Technology Division (PSTD) executive committee of the American Vacuum Society (AVS)

Editor of Microelectronics Engineering and of Micro Nano Engineering scientific journals

Dr. Darnon has been a member of the Continuing Education Institute-Europe faculty since 2011. He is the CEI-instructor on plasma etching for in-house classes at TEL, ASML, Intel, Analog Devices and others.